DESIGN AND ANALYSIS OF A FIRST-ORDER SIGMA-DELTA CONVERTER WITH CMOS-MEMS DIFFERENTIAL CAPACITIVE SENSOR

BY

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A dissertation submitted in fulfilment of the requirement for the degree of Master of Science (Electronics Engineering)

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JANUARY 2012

ABSTRACT

This dissertation presents the design and analysis of a MEMS accelerometer and its accompanying interface circuitry. The interface circuit is a sigma-delta (Σ-Δ) analog-to-digital converter (ADC) which is capable of converting an analog low voltage (in mV range) and low frequency signal into digital signals. The first-order 1-bit Σ-Δ ADC is designed and simulated using MATLAB® and Cadence™ Spectre design tools. Σ-Δ converters are preferred for MEMS applications due to its capabilities of processing low output voltages from MEMS sensors and its noise-shaping techniques which push the noise outside the bandwidth of the baseband signals. The MEMS accelerometer is designed as a CMOS-MEMS differential capacitive sensor. The usage of CMOS technology to form the sensor allows integration of the MEMS sensor with its ADC interface circuitry together on the same chip. Each component in the converter is designed and simulated separately using Silterra 0.13um CMOS process technology. Simulation results indicate agreement with the theoretical evaluations.

خلا صة

إن هذا البحث – بتوفيق الله تعالى– يقدم تصميم وتحليل دائرة التفاعل مع والتردد المنخفض " MEMS " الاستشعار. فوظيفة الدائرة هي لتحويل الإشارات التناظرية إلى إشارات رقمية (ADC)، وجهاز استشعار السعة التفاضلية مع تصميم متكامل معا، باستخدام برامج المحاكاة " MATLAB® " وشبح " Cadence™ Spectre ". وتم تصميم الطاقة المنخفضة من الدرجة الأولى (واحد بت سيغما دلتا) " Σ-Δ ADC ". وقد تم تصميم كل عنصر في المحول الأول ومحاكاة بشكل منفصل باستخدام برنامج " CMOS 0.13µm " للشركة Silterra. وبعد ذلك كله، هو بناء الدوائر والمحاكاة، ويرد استشعار متوافقة " CMOS-MEMS " التفاضلية بالسعة التي تستخدم؛ لاختبار التغيرات المفاجئة من تسارع باستخدام نفس " CMOS "التكنولوجيا العملية، وهو يتم عن طريق محاكاة نموذج " COMSOL Multiphysics® ". ومن نتائج المحاكاة والاستشعار دوائر الاستشعار التفاضلية بالسعة ممتازة مع الجهد الناتج الخطية ، بينما يمكن تحويل الطاقة شركة تطوير العقبة Σ-Δ استهلاك الجهد المنخفض به من دقة عالية جدا للإشارات الرقمية . وعلاوة على ذلك، فإن استخدام تحليل نطاق تردد كثافة القدرة الطيفية، أي "PSD "، التحقق من أن التردد المنخفض " Σ-Δ ADC " مهام لجنة المساعدة الإنمائية ، وحساب اشارة الى نسبة الضوضاء (SNR).

APPROVAL PAGE

I certify that I have supervised and read this study and that in my opinion; it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Master of Science in Electronics Engineering.

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DECLARATION

I hereby declare that this dissertation is the result of my own investigations, expect where otherwise stated. I also declare that it has not been previously or concurrently submitted as a whole for any other degrees at IIUM or other institutions.

Ma Li Ya

Signature:…….. Date:……..

INTERNATIONAL ISLAMIC UNIVERSITY MALAYSIA

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Affirmed by Ma Li Ya

…….. ……..

Signature Date

To my beloved parents, brother, grandparents, and all Muslim Ummah…

ACKNOWLEDGEMENTS

Praise be to Allah (S.W.T.), the Almighty for bestowing His Grace and Mercy, Solawat and Salam to our beloved prophet (P.B.U.M).

At the very outset, all my prayers and thankfulness to Almighty Allah for abilities in granting me the opportunity with His Great Blessings to carry out and accomplish this dissertation successfully throughout the years of my achievement for seeking the knowledge.

I wish to express my deepest gratitude to my supervisor, Assoc. Prof. Dr. Sheroz Khan for permitting me to carry out this thesis with his guidance. I take immense pleasure in expressing my heartfelt gratitude to my co-supervisor, Assist. Prof. Dr. Anis Nurashikin Nordin. Since her inspiration, guidance, valuable suggestion and assistance, it can help me to complete this research within proper time.

I offer my appreciation to my lecturers and members in Electrical and Computer Engineering Department; Prof. Dr. Momoh J. E. Salami, Prof. Dr. Othman O. Khalifa, Prof. Dr. A.H.M. Zahirul Alam, Assoc. Prof. Dr. Muhammad Ibn Ibrahimy, Assoc. Prof. Dr. Aisha Hassan Abdalla Hashim, and Assist. Prof. Teddy Surya Gunawan who offered the related electronic classes and helped me during the research. I also gratefully acknowledge to CPS who gave me the Ummatic scholarship and IIUM Research Management Center who supplied the research grant which can make me to finish my master study successfully. I also appreciate the advice of everybody that I could not mention personally one by one for their encouragement and critical comments which enabled me to notice the weaknesses of my dissertation and make the necessary improvements.

And of course, I extend my thankfulness to all my friends; Aliza Aini, Atika Arshad, Nurul Arfah, Iffah Che Omar, Siti Farah, Li Wen Jun, and to everybody who played an important role in my success, guiding me in the right direction. Their encouragement and help made me confident to fulfilling my desire and overcoming every difficulty encountered.

Last but not least, I am very grateful to my father: Ma Qi, my mother: Tao Yu Ling, my brother: Ma Li Jia, my grandparents: Ma Cun Cai and Tao Shu Qin, my uncle: Ma Cheng, for their understanding and their love, encouragement to work hard and to continue pursuing my masters. Their firm and kind-hearted personalities have made me steadfast and not bend to difficulty. Their prayers to Allah for my success and pride in me motivated me to work harder and do my best. Their love and support made me strong to undertake and complete my Masters. I own my every achievement to all of them.

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LIST OF ABBREVIATIONS

VLSI	Very Large Scale Integration
ADC	Analog-to-Digital Converter
PCM	Pulse Code Modulation
SNR	Signal-to-Noise Ratio
MEMS	Micro-Electro-Mechanical System
IC	Integrated Circuit
CMOS	Complementary Metal-Oxide-Semiconductor
DAC	Digital-to-Analog Converter
RMS	Root Mean Square
STF	Signal Transfer Function
NTF	Noise Transfer Function
ISDN	Integrated Services Digital Network
OSR	Oversampling Ratio
ENOB	Effective Number of Bits
MOSIS	Metal-Oxide-Semiconductor Implementation Service
RDC	Resistance-to-Digital Converter
SCI	Switched-Capacitor Integrator
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NMOS	N-Channel MOSFET
PMOS	P-Channel MOSFET
OP AMP	Operational Amplifier
SPICE	Simulation Program with Integrated Circuit Emphasis
UTM	Ultra Thick Metal

DRIE	Deep-Reactive-Ion Etching
FFT	Fast Fourier-Transform
BIST	Built-In-Self-Test
PDK	Process Design Kid

LIST OF SYMBOLS

Σ-Δ	sigma-delta
f_s	sampling frequency
f_B	base band frequency
σ_e	the rms value of the quantization error
$H_x(z)$	signal transfer function
$H_e(z)$	noise transfer function
σ_{ey}^2	base band noise power
T_s	sampling period
Φ_1 (Φ_2)	non-overlapping clock
Q	capacitor's charge
H(z)	the transfer function of the integrator
$V_{tn}(V_{tp})$	MOSFET threshold voltage
(W/L)	MOSFET's width over length
$V_{dd}(V_{ss})$	whole chip power supply
$V_{ref1}(V_{ref2})$	reference voltage
ε_0	the electric constant
ε_r	the capacitor's relative static permittivity
a	acceleration
g	acceleration due to gravity ($1g=9.8m/s^2$)
U_E	energy in electronic element
E	electric field

CHAPTER ONE

INTRODUCTION

1.1 BACKGROUND

Sensors are fundamental elements in all the instruments and circuits employed for measurement and monitoring purposes. They are extensively applied for measurement and control both in scientific and industrial fields. With the development of circuit and fabrication technology, particularly with the advances in very large scale integrated (VLSI) technology it has been possible that both sensors and the electrical signal-processing circuitry to be placed on the same chip resulting in reduced size and parasitic effects.

An analog-to-digital converter (ADC) is a signal-processing circuit, which produces an ideal digital output from an analog input. Conventional ADC suffers from inherent quantization errors which result from the fact that a signal sample is assumed to be of the same quantity over its entire sampling interval (Tropp, et al., 2010). The larger the number of bits produced by an ADC in the digital output, the smaller the quantization error, but at the cost of a more complex circuitry.

ADCs can be typically categorized into two types, (i) conventional ADCs and (ii) oversampling ADCs (Aziz, et al., 1996). Each type has its own advantages and disadvantages, according to their circuit's sample and hold delay, quantization error and speed. Most of the conventional ADCs, such as the successive approximation converter, sub ranging or pipelined converter, and flash converter types quantize signals sampled at (or slightly above) the Nyquist rate $\left(f_s = 2 f_B\right)$ (Aziz, et al., 1996). These converters are usually called as Nyquist rate pulse code modulation (PCM)

converters. The other set of converters, such as sigma-delta (Σ-Δ) converter, is basically an oversampling converter. Such converters operate much faster than the Nyquist rate converters (typically 20 to 512 times faster) with an increased signal-to-noise ratio (SNR) by filtering out quantization noise that is not in the signal's bandwidth (Johns & Martin, 1997). Figure 1.1 shows the tradeoffs between the signal bandwidth and the output of conversion resolution of some ADC techniques.

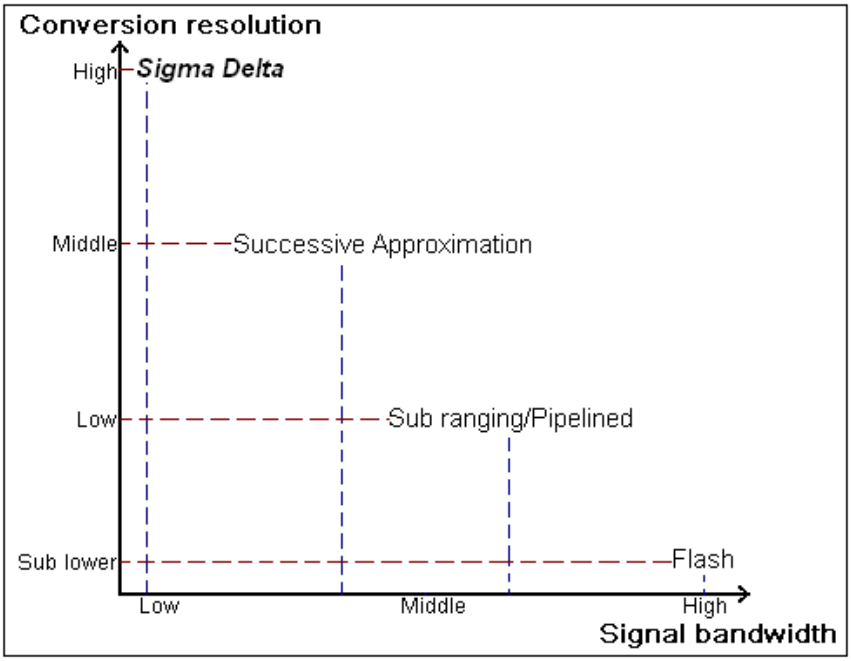

Figure 1.1: Bandwidth and resolution tradeoffs (Aziz, et al., 1996).

Figure 1.1 illustrates that a Σ-Δ converter can provide the highest conversion resolution, using very low frequency bandwidths. These properties are properly suited for converting signals from the micro sensors, such as micro-electro-mechanical system (MEMS) sensors, or biomedical sensors.

A MEMS sensor's output is characterized by its slow varying outputs with frequencies ranging from 10Hz to 200 kHz and its magnitude in the order of some

micro (or milli) volts. This type of signal has a larger chance to be corrupted by field (or noise) external to it. The usage of a high resolution ADCs is especially important for processing of signals rich in contents where even quantization error loss of the signal is considered to be an unaffordable element.

The Σ-Δ converter is a popular signal conversion technique for obtaining high resolution digital output of an input signal with relatively small bandwidth. It performs noise-shaping where the noise function is forced to have low magnitude at the baseband and higher magnitudes at high frequencies (Aziz, et al., 1996). Σ-Δ topology does not limit the number of bits, but the cost is exponentially raising dependent on the number of bits produced. It requires small bit (1-bit or 2-bit) internal quantization. This allows the quantizer to be realized as a 1 or 2-bit comparator, leading to considerably simplified analog circuitry. It also has inherent linearity and high tolerance to sources of errors stemming from circuit imperfections (Abbiati, et al., 2004).

1.2 PROBLEM STATEMENT AND ITS SIGNIFICANCE

An ADC is used to obtain the digital equivalent of a given data carrying analog signal derived from a transducer. This conversion is required to be as error free as possible. Once digitized, the signals can be efficiently transmitted as compared to its analog partner that may suffer from losses. Also, a digitized signal is easy to be stored with no error and simple use of electronics. Small size, low cost, and high resolutions are desirable features to be achieved during the conversion process.

For Nyquist rate converters (or traditional converters), each signal sample is quantized at the full precision or resolution of the converter. This kind of converters essentially obtains output by comparing the input voltage to various reference levels.

The resolution of such converters implemented on VLSI chip is limited by the technology on which these chips are fabricated (Aziz, et al., 1996). These samples, for example are quantized by the digital code from 000 to 111 in the case of a three-bit ADC, in other words a given analog signal sample is regarded as one out of eight levels. As such samples are being categorized by resistive and capacitive elements, any mismatch in the resistors or capacitors results in loss of conversion accuracy. For an n-bit resolution converter, the number of matching components is at least 2^n samples. The realization of accurate resistive and capacitive values in VLSI technology is a challenging task and an extremely high cost, especially in case of for high resolution requirement. However, for oversampling Σ-Δ converters, they employ only a simple two-level quantizer, embedded within a feedback loop (Norsworthy, et al., 1996). This technique makes such converters especially insensitive to circuit imperfections and components mismatching. That means using current integrated circuit technology to attain high resolution Nyquist rate converters is a real challenging task in chip fabrications.

This work intends to integrate the oversampling ADC together with a MEMS sensor on the same chip. There have been several reported designs focusing on Σ-Δ modulators, such as those reported in (Nordin & Zaghloul, 2002) and (Park & Perrott, 2009). They use different processing, and are fabricated in 1.6μm CMOS technology (Nordin & Zaghloul, 2002) and in 0.18μm CMOS as in (Park & Perrott, 2009). The works in (Amini & Ayazi, 2004) and (Oysted & Wisland, 2005) are the designs of Σ-Δ converter with sensor together, their CMOS technology and power supply make them not to be the best choice. In order to make the integrated circuit (IC) area smaller with less power consumption, as well as less chip cost, the smaller design technology with the minimum voltages supply is required.

The significance of this work lies in its application in cases where the signal of interest is too weak to be retrieved in full. The design consists of two major blocks: a CMOS-MEMS differential capacitive sensor and a Σ-Δ ADC, which are worked out together on a single chip and implemented in Silterra 0.13um CMOS standard technology. The MEMS differential capacitive sensor designed here is used in accelerometers and similar pressure sensing devices such as air bag used as an impact detecting device. The primary significance of this work lays on the improved resolution, reduced power supply design and chip design dimensions.

1.3 RESEARCH OBJECTIVES

This dissertation focuses on the design and analysis of a novel on-chip Σ-Δ converter integrated with a MEMS differential capacitive sensor in 0.13μm CMOS (complementary metal-oxide-semiconductor) technology. The novelty of this work lays in the integration of the Σ-Δ ADC and the MEMS sensor on the same chip. Full integration eliminates bond-wire parasitic which results in noise minimization and shrinking of the device size. The objectives of this work are summarized as follows.

i. To design a MEMS differential capacitive acceleration sensor using Silterra's 0.13μm CMOS process.
ii. To design a first-order 1-bit Σ-Δ ADC based on 1.2V Silterra's 0.13μm CMOS technology, using MATLAB and Cadence.
iii. To integrate the developed ADC with the on-chip MEMS sensor.
iv. To evaluate the performance of the developed ADC with respect to the following parameters: linearity, resolution, noise immunity and power consumption.