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DEVELOPMENT OF AN EFFECTIVE ALGORITHM FOR MICROCHIP LEAD INSPECTION

BY

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ABSTRACT

A new effective method for the microchip lead inspection for the chip manufacturing industry has been developed in this research. This new technique is implemented using Lab View programming environment and tested on many sample images using National Instruments frame grabbers and hardware interfaces. The first part of the software deals with the image enhancement and auto-thresholding method to prepare for precision measurements. The second part of the software is using newly developed statistical analysis technique for automatic IC leads defect detection (such as linearity, implied planarity, offset...etc). Finally the research carries out a precision, repeatability and reproducibility test procedures of the system. Contrary to the gray scale pattern matching technique, the proposed technique employs selected parameters of binary blobs to perform fault detection and measurements. This leads to a significant reduction of image processing time. A special combination of gray level filtering techniques with gray morphological operations has been used to enhance the borders of the lead images. A newly developed threshold calibration technique significantly improves the measurement accuracy. A unique statistical analysis has been developed to identify all possible lead defects in the chips. This method is rotationally and scale invariant and able to detect defective leads for the chips with different specifications. The minimum required information about the microchip is the number of leads.

ملخص البحث

لقد طور هذا البحث طريقة فعالة وجديدة لفحص أرجل الرقائق الإلكترونية صنعيها. وهذه التقنية ا ديدة قد جهزت باستخدام لغة الـ ة (Lab View) وقد فحص من خلال هذه التقنية العديد من العينات الصورية باستخدام لاقط (NI) الصوري ا رتبط بعدة أدوات أخرى. ا زء الأول من ا نامج يعمل على سـ خاصية الصورة، و توي على تقنية الـ (Autothesholding) ا تعمل على تدقيق القياسات. وا زء الثا من هذا ا نامج يعمل على التحليل الإحصائي بطرية جديدة ومطورة للكشف عن عيوب أرجل الرقائق الالكترونية أوتوماتيكياً مثل: (بعد القدم الضم أو ا طي عن مستواه الأصلي أو الا راف الأفقي ا). وأخ اً يعرض هذا البحث إجراءات فحص الدقة و التكرار والتحصيل للنظام. با قارنة مع تقنية مطابقة الطبقات الرمادية فإنّ التقنية ا قترحة هذا البحث تعمل صائص معينة من الـ (Binary Blobs) للقيام بكشف الأخطاء وإ اد القياسات ا طلوبة، ا يؤدي إ تقليص وقت معا ة الصورة. وقد دمج التقنيات ا عملية للتصفية الرمادية مع الـ (Morphological) الرمادية لتحسـ صورة يط رجل الرقيقة الالكترونية.و التحليل الإحصائي الآنف ذكره أدى إ تطوير طريقة التعرف على يع العيوب ا تملة بأرجل الرقائق الالكترونية. وهذه الطريقة دورا نية بقياسات متعددة قادرة على كشف عيوب أرجل الرقائق الالكترونية ذات ا قاييس ا ختلفة. وبناء على ذلك فان ا دخل ا طلوب للنظام هو عدد أرجل الرقيقة الالكترونية فقط.

APPROVAL PAGE

I certify that I have supervised and read this study and that in my opinion; it confirms to acceptable standards of scholarly of presentation and is fully adequate, in scope and quality, as a thesis for the degree of Master of Science in Mechatronics Engineering.

Nazim Mir-Nasiri
Supervisor

I certify that I have supervised and read this study and that in my opinion; it confirms to acceptable standards of scholarly of presentation and is fully adequate, in scope and quality, as a thesis for the degree of Master of Science in Mechatronics Engineering.

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This thesis has been submitted to the Kulliyyah of Engineering and is accepted as a partial fulfillment of the degree of Master of Science in Mechatronics Engineering.

Ahmad Faris Ismail
Dean, Kulliyyah of Engineering

DECLARATION

I hereby declare that this thesis is the result of my own investigation, except otherwise stated. Other sources are acknowledged by footnotes giving explicit references and a bibliography is appended.

Name: Haitham Hilmi Lutfi Al-Obaidy

Signature:………………………………….. Date: …………………………………..

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Signature   Date

"To my beloved parents with gratitude for their pray and support…

To my great teacher and father Hilmi Lutfi Al Obaidy for his guidance and support…

To all my brothers and sisters…"

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LIST OF ABBREVIATIONS

ADC	analog-to-digital converter
APP	appendix
BGA	ball grid array
BLOB	binary large object
BNC	bayonet nut connector
CCD	charge coupled device
CCIR	international radio consultative committee
DIL	dilation
DIP	dual in-line package
DSP	digital signal processor
ERO	erosion
Etc	et cetera
FOV	filed of view
HSL	hue saturation and luminance
HSYNC	horizontal sync
IC	integrated circuit
ICLI	integrated circuit lead inspection
IEEE	institute of electrical and electronics engineers
LED	light emitting diode
LQFP	low profile quad flat package
LSI	electronics large-scale integration
NI	national instruments
NTSC	national television standards committee

OP	opening
PAL	phase alternation line
PCB	printed circuit board
PCI	peripheral component interconnect
QFP	quad flat package
RGB	red green and blue
ROI	regions of interest
RS	recommended encoding standard
R&R	repeatability and reproducibility
RTSI	real-time system integration
SDIP	shrink dual-in-line package
SMD	small manufactured devises
SMT	scanning measurement technology
SOJ	small outline J-lead
SOP	small out-line package
SSOP	shrink small outline package
TQFP	thin quad flat package
TSOP	thin small outline package
VHDCI	very high density cable interconnect
VSYNC	vertical sync
ZIP	zig-zag in-line package

CHAPTER 1

INTRODUCTION

This chapter describes the contents of thesis and research conducted for development of an effective algorithm for microchip lead inspection. Thesis statement and significance of this research are given followed by research objectives and steps taken to accomplish these objectives. The last section of this chapter is an outline of this entire thesis with brief summary of each chapter provided.

1.1 Introduction

As a progress is continually being made in inspections, there is corresponding need for the use of machine vision in these processes. Therefore the outcome of this research is directly related to development of new machine vision system. Machine vision system is to create a model of the real world from images, to recover useful information about a scene from its two-dimensional projection. Since images are 2-D projection of the 3-D world, the information is not directly available and must be recovered. This recovery requires the inversion of a many –to-one mapping. To recover the information, knowledge about the objectives in the scene and projection geometry is required. Machine vision system helps a physician to recover information by enhancing the images. Quantitative measurements on regions of interest can also be made easily available. Such a system is being developed for all image modes useful in different aspects of health care. Similar applications are being developed for inspection of industrial, agricultural, and other products. Machine vision systems have been used for quality control of products ranging from pizza to turbine blades, and from submicron structures on wafers to auto-body panels.

1.2 Thesis Statement

The manufacturing process for surface mounted integrated circuits (IC) consists of wafer fabrication and chip packaging. The chip-packaging processes consist of sawing the die from the wafer, die bonding, wire bonding, molding, trimming and forming, marking, plating, and inspection. The trend toward miniaturization, higher pin counts and finer pitches have put a lot of stress on both the IC manufacturing processor and the inspector. In order to streamline the entire IC production system and to relieve inspector stress, it is necessary to inspect these components automatically based on computer vision systems. Inspection of an IC lead during IC packaging and printed circuit board assembly may include the following categories: Missing or extra leads, lead Planarity or linearity, lead offset, and lead pitch.

Automated vision system for IC lead inspection can be accomplished either using *pattern-matching or blob analysis.* Most of the industrial lead inspection systems are using *pattern-matching* technique that locates regions of a grayscale image for matching a predetermined template. Pattern matching technique is able to find template matches regardless of poor lighting, blur, noise, shifting or rotation of the template but it is quite time-consuming and computationally expensive. The system developed in this research is dealing with inspection of microchip leads using *blob analysis* technique; the blobs are areas of touching pixels within an image, in which all pixels have the same logical state. All pixels in an image that belong to a blob are in a foreground state. All other pixels are in a background state. In other words, it is a binary image where pixels in the background have values equal to zero while every non-zero pixel is part of a binary object. In this thesis, blob analysis is used to find different statistical information about the IC leads to measure some of the critical lead dimensions. Blob generation and analysis increase the processing speed and easily handle blur and noisy images.

In this thesis, *blob analysis* employs selected parameters of binary blobs to perform fault detection and measurements for IC lead. A new effective mathematical algorithm is developed and then evaluated by some of the commercially available vision platforms which can offer a wide variety of image acquisition and processing tools. The results for reliability of leads measurement of the proposed system are presented. The performance of the system is discussed and precision, repeatability and reproducibility test procedures are conducted for obtained measured data.

1.3 Research Objectives

i. To develop an effective and autonomous microchip inspection system based on blob analysis technique.
ii. To develop new auto-thresholding for precision microchip image measurements.
iii. To develop new statistical algorithms to enhance reliability of the vision inspection system, by making this system rotational and scale invariant and perform simulation studies of the developed model using Lab-View IMAQ tools.
iv. Design and construct image frame grabber to study and verify the performance of the proposed algorithm using National Instrument image acquisition. Conduct a field test of the system for accuracy, repeatability and reproducibility using semiconductors manufacturer's standard procedures.

1.4 Methodology

i. The research started with an identification and classification of lead defects in IC packages and studying existing lead inspection systems in the market and industry.

ii. Hardware setup and image calibration for monochrome (gray) image acquisition using NI-IMAQ vision builder.

iii. Collecting sample chip images for blob analysis and examining the images using NI-IMAQ vision builder.

iv. Apply different image processing techniques such as image Filtering and gray morphology for image enhancement.

v. Development of auto-thresholding technique for generation of blobs from sample gray images.

vi. Develop an algorithm for recognizing defects in IC packages leads and calculating their critical measurements. Simulate the algorithm using Lab-View.

vii. Conduct real field measurement and perform system repeatability and reproducibility study.

1.5 Thesis Outline

i. Chapter 2: This provides the background information on the Microchip Lead Inspection research. It gives a theoretical background on image processing techniques and areas of their applications. IC package leads inspection strategies and comprehensive literature reviews of related research topics are also presented.

ii. Chapter 3: It focuses on image system setup and calibration, this chapter describes how to setup an imaging system and calibrate it so that one can convert pixel coordinates to real-world coordinates for making accurate measurements from acquired images.

iii. Chapter 4: This chapter discusses the development of Image processing using blob analysis techniques. It provides a sequence of image processing techniques to enhance the quality of IC leads images, a typical blob analysis process that scans through an entire IC package image and detects all the particles, or blobs which represent the leads in the image and builds a detailed report on each such particle.

iv. Chapter 5: This chapter discusses the development of algorithms for recognizing defects in IC packages leads. These algorithms were tested for different IC lead defects to ascertain their ability to inspect and provide measurements of leads critical dimensions, the critical dimensions of the leads is compared with the measured ones.

v. Chapter 6: This chapter focuses on presenting the results obtained from the above experimental setup. A mathematical average and range method is used to estimate both repeatability and reproducibility for the system.

vi. Chapter 7: Presents the conclusion obtained from the research conducted on Development of An Effective Algorithm for Microchip Lead Inspection. Also summary of this research is given along with the recommendation for future work.

CHAPTER 2

LITERATURE REVIEW

The chapter discusses some background on machine vision, IC package defects over view and brief explanation of related theory, image processing techniques for different approaches of inspection. Finally, various related IC package inspection strategies for Lead defects are explained.

2.1 Related Works

One of the recent works, [Tung, 2001] proposed an automated vision system for inspection SOP (Small Out-line Package) or DIP (Dual In-line Package) IC lead flaws. This system consists of a special lighting and image acquisition system, and a series of processing techniques to measure the lead coplanarity and to inspect skewed lead frames. First, a SOP or DIP device image is captured using a top-view CCD (Charge Coupled Device) camera and LED (Light Emitting Diode) ring type lighting through a special layout that uses two mirrors at the sides of the reference plane at 45^o. The image contains the top view of the IC and the reflection of the IC lead height. The proposed image acquisition system provides the opportunity to inspect the IC leads and marks simultaneously using the same image. An image correlation procedure is used in the IC lead inspection system to find the coordinates of the IC leads. A new algorithm for determining the reference plane of an IC and measuring the coplanarity is proposed and compared with a traditional algorithm, however this system seems to be costly and concentrate only on coplanarity defects.

In [Stanke, 1998] a layout of four mirror planes and a backlighting source to inspect all of the sides of a QFP (Quad Flat Package) from one point of view has been developed. The mirrors were located at the four sides of the reference plane at a 45º, causing a reflection of the light rays, so that all sides could be seen directly from above. The coplanarity algorithm involved measuring the width of the light gaps and returning Boolean information about the coplanarity of the pins. Although this system proved to be précised and robust and was integrated into a SMD-device (Small Manufactured Devises) industrial process, the IC chip had to be placed onto a carrier and then put on a specially designed layout.

[Smeyers & Truyens, 1992] designed a special lighting technique and an advanced subpixel technique (HALE) to measure the lead coplanarity for a Quad Flat Package (QFP) IC. They used four different light sources around the four corners of the QFP and a camera to capture the lead image. For every lead, two light sources in different positions were used to create two projected images of the lead on a frosted glass plate. The respective positions of the same lead in the two images were then used to calculate the position and the height of the lead. The light sources were switched sequentially, producing four different images. All of the information for the four images was then combined into a data structure containing the position of all of the individual leads. Since the system measured the coplanarity based on projecting images and a triangulation technique, a calibration procedure had to be conducted.

[Takafumi & Masayasu, 1993] a system that has been developed for the final visual inspection of LSI packages. The system consists of an image input method and hardware that is capable of high-speed processing to inspect the large number of items in the final inspection, and developed software that can inspect for different package defects. The image is captured using a 2048 x 2048 CCD pixel and 60 mm filed of