DESIGN AND DEVELOPMENT OF IN SITU FPGA-BASED WATER QUALITY MONITORING KIT

BY

ABDULRAHMAN BAHAA ZAIDAN

A dissertation submitted in fulfilment of the requirement for the degree of Master of Science in Computer and Information Engineering

> Kulliyyah of Engineering International Islamic University Malaysia

> > November 2022

ABSTRACT

In 2017, about 144 million people collected water from untreated water bodies, such as lakes, streams, and rivers. One of the major causes of death is consuming contaminated or polluted water. Measuring and monitoring water quality are usually done using two methods. The conventional method occurs by taking samples of water and then transferring them to the laboratory. The second method is real-time water quality by integrating the Internet of Things (IoT). This method is preferable as it only requires smart sensors and processors to monitor the water quality. Among the widely used processors are the Arduino and Raspberry Pi. However, these two processors have a limitation, including a limited number of hard-coded input/output pins, unlike the Field Programmable Gate Array (FPGA) processor, which has many input/output pins not hard-coded to allow different interfacing of multiple sensors. Based on the literature, an FPGA platform provides more flexibility and reconfigurability features when compared with the Arduino and Raspberry Pi. This research mainly focuses on designing a reconfigurable multi-core Smart Water Quality System (SWQS) measuring the pH, Total Dissolved Solids (TDS), and turbidity parameters. The hardware design was developed based on the system-on-chip (SoC) design methodology on an FPGA to parallelize the SWQS functionality. A Liquid-Crystal Display (LCD) display has been incorporated into the Raspberry Pi to show real-time data. The Platform Designer on Ouartus II has been used to instantiate four cores to integrate all functions into one processor. The Eclipse tool on Quartus II, on the other hand, was used to program the sensors using embedded C language. The proposed design has been implemented on DE10 Nano FPGA-SoC consuming 9% of logic resources and 57% of internal memory. To verify the proposed system functionality, the sensors were tested on different liquids. To test the pH level, the pH sensor was tested on pure water, lemon juice, and milk to show the acidity and alkalinity. The pH sensor showed 7, less nearly 2, and less than 8 for pure water, lemon juice, and milk, respectively. The TDS sensor successfully detected the salt added to the water, and the TDS values increased to approximately 1800 ppm. Finally, the turbidity sensor revealed the dust inserted in the solution. The more dust in the liquid, the more TDS value there was recorded. Additionally, results showed that the processing time of all the sensors using FPGA is approximately 300 ms for ten readings; on the other hand, the processing time of using other processors, such as Arduino, took 2 s for ten readings. This is because FPGA is functioning at 100 MHz, while Arduino's frequency is not more than 24 MHz. All real-time sensor readings were shown on a Linux Terminal. In conclusion, the proposed FPGA-based system can be utilized as a heterogeneous multi-core system for many applications, including the SWQS.

ملخص البحث

اكثر من مائة واربع واربعون مليون انسان ياخذون احتياجاتهم من المياه من مصادر غير معالجة مثل الانحار والبحيرات .في بعض الدول النامية ,معظم المصانع تقوم برمي الفضلات في المياه وهذا يجعل المياه بالقرب من المصانع اكثر تلوثا لأنها تحمل مواد كيميائيه بالأضافه إلى المواد الثقيلة .هذه المواد تؤثر بشكل سلبي على البيئة وعلى الكائنات الحية التي تعيش في المياه لان المواد الثقيلة تنشر الفايروسات والبكتيريا .في هذه الايام يتم قياس جودة المياه بطريقتين هما اما الطريقة التقليدية وهي عبارة عن اخذ عينات من المياه ونقلها الى المختبر ومن ثم قياس جودتما ,ولكن هذه الطريقة تحتاج الى وقت وتكلفه اكثر .بالاضافة الى ذلك , حالة المياه من الممكن ان تتغير خلال عملية النقل .اما الطريقة الثانية فهي قياس جودة المياه بأستخدام الحساسات الذكية مع المعالجات ونقل البيانات بطرق مختلفة .هذه الطريقة مفضلة بشكل أكبر من الطريقة التقليدية لانها فقط تحتاج إلى الحساسات الذكية بالاضافة إلى المعالج لقياس جودة المياه في كل وقت . هذه الطريقة ستساعد المستخدم على اتخاذ القرار بسرعة في الحالات المفاجأة .لهذا فأن هذا المشروع يركز بشكل اساسى على استخدام حساسات لقياس الأس الهيدروجيني والعكورة بالأضافة الى كمية المواد الذائبة .بعد ذلك تقوم مصفوفة البوابات المنطقية القابلة للبرمجة بمعالجة البيانات وارسالها لأجل عرضها على الشاشة .هذا المشروع سيقلل من تعقيد الأجهزة الأخرى المستخدمة في قياس جودة المياه .وسوف تقوم بأستخدام الأجهزة مع البرمجة لتقليل الوقت المستخدم في تطوير جهاز متحسس المياه الذكي .اخيرا وليس اخرا ,جهاز الراسبري باي سيستخدم فقط لعرض البيانات على الشاشة المتربطة به .سيقوم معالج الراسبري باي بأستلام البيانات عن طريق تطبيق مبرمج بداخله ومن ثم عرضها على الشاشة .الجهاز المصمم قدتم اختباره على سوائل مختلفة مثل المياه النقية ,عصير الليمون ,الحليب لقياس الأس الهيدروجيني .

اما نسبة العكورة فقد تم استخدام المياه النقيه بالاضافه الى مياه مع القليل من الرواسب ومياه مع الكثير من الرواسب. اخيرا فقد تم استخدام المياه النقية ومياه تحتوي على الملح لقياس المواد المذابة في الماء. عن طريق هذا المشروع يمكن استخدام البيانات عن طريق ربطها ببرامج اتخاذ القرار, تحليل البيانات وغيرها من البرامج.

APPROVAL PAGE

I certify that I have supervised and read this study and that, in my opinion, it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Master of Science Engineering.

Binti Azman Ameli Super

Huda Adibah Mohd Ramli Co-Supervisor

I certify that I have read this study and that, in my opinion, it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Master of Science Engineering..

100011111	azuin Ab. Examine	 	• • • • •

Suriza Ahmad Zabidi Internal Examiner

This dissertation was submitted to the Department of Electrical and Computer Information and is accepted as a fulfilment of the requirement the degree of Master of Science Engineering.

> Rafiqul Islam Head, Department of Electrical and Computer Information Engineering

This dissertation was submitted to the Kulliyyah of Engineering and is accepted as a fulfilment of the requirement for the degree of Master of Science Engineering.

Sany Izan Ihsan Dean, Kulliyyah of Engineering

DECLARATION

I hereby declare that this dissertation is the result of my investigations, except where otherwise stated. I also declare that it has not been previously or concurrently submitted as a whole for any other degrees at IIUM or other institutions.

Abdulrahman Bahaa Zaidan

fra
Signature

Date 2022/12/05

INTERNATIONAL ISLAMIC UNIVERSITY MALAYSIA

DECLARATION OF COPYRIGHT AND AFFIRMATION OF FAIR USE OF UNPUBLISHED RESEARCH

DESIGN AND DEVELOPMENT OF IN SITU WATER QUALITY KIT

I declare that the copyright holders of this dissertation are jointly owned by the Student and IIUM.

Copyright © 2022 Abdulrahman Bahaa Zaidan and International Islamic University Malaysia. All rights reserved.

No part of this unpublished research may be reproduced, stored in a retrieval system, or transmitted, in any form or by any means, electronic, mechanical, photocopying, recording or otherwise without prior written permission of the copyright holder except as provided below

- 1. Any material contained in or derived from this unpublished research may only be used by others in their writing with due acknowledgement.
- 2. IIUM or its library will have the right to make and transmit copies (print or electronic) for institutional and academic purposes.
- 3. The IIUM library will have the right to make, store in a retrieval system and supply copies of this unpublished research if requested by other universities and research libraries.

By signing this form, I acknowledged that I have read and understand the IIUM Intellectual Property Right and Commercialisation policy.

Affirmed by Abdulrahman Bahaa Zaidan

2022/12/05

Signature

Date

ACKNOWLEDGEMENTS

First and foremost, I would like to thank Allah for blessing me each and every day. Thanks for the strength, wisdom, and faith to make it through life's everyday challenges.

I would like to thank my parents. There are so many things that I want to thank them for. They are the reason behind all of my success, and I am forever indebted to them. I would especially like to thank Associate Professor Amelia Wong Binti Azman for her outstanding guidance, advice, inspiration, and encouragement throughout my research progress. It is my greatest honor to work under her supervision. Thank you for nurturing me into a hard-working student and for all your patience and guidance. You were more than just supervisors to me. I am deeply indebted to you.

In addition, my gratitude goes to my beloved, lovely wife; for her prayers, understanding, and endurance while away.

Finally, I want to thank Fawaz Mohammed for his countless midnight calls and messages just to do this research; I am so grateful and thankful to you. I am very thankful for all of the above for being the solid support system in my life. Thank you. Allah blesses you

Once again, we glorify Allah for His endless mercy on us, one of which is enabling us to successfully round off the efforts of writing this thesis. Alhamdulillah.

TABLE OF CONTENTS

Abstract	ii
Abstract in Arabic	iii
Approval Page	v
Declaration	vi
Copyright Page	vii
Acknowledgements	viii
Table of Contents	ix
List of Tables	xii
List of Figures	xiii
CHAPTER ONE: INTRODUCTION	
1.1 Overview	
1.2 Research Background	
1.2.1 Field Programmable Gate Array (FPGA)	
1.2.2 Heterogeneous System Architecture (HSA)	
1.3 Problem Statement	
1.4 Research Objectives	
1.5 Research Scope	
1.6 Dissertation Layout	
1.7 Summary	7
CHAPTER TWO: LITERATURE REVIEW	
2.1 Overview	
2.2 Different Water Quality Approaches	
2.2.1 Conventional Approach	
2.2.2 Internet of Things (IoT) Approach	
2.3 Sensors Used in Monitoring Water Quality Parameters	
2.3.1 pH Sensor	
2.3.2 Temperature Sensor	
2.3.3 Turbidity Sensor	
2.3.4 Conductivity Sensor	14
2.3.5 Dissolved Oxygen Sensor	
2.3.6 Total Dissolved Solids (TDS) Sensor	16
2.3.7 Free Chlorine Sensor	16
2.3.8 Water Level Sensor	
2.4 Related Research	
2.4.1 Arduino as a Processing Platform	
2.4.2 Raspberry Pi as Processing Platform	26
2.4.3 TI CC3200 as Processing Platform	30
2.4.3.1 FPGA as Processing Platform	
2.4.4 Other Processing Platforms	
2.4.5 Summary of Related Works	
2.5 Proposed FPGA-Based SWQS	
2.6 Understanding The FPGA-SoC Heterogeneous system	
2.6.1 FPGA Chip	
2.6.2 System-on-Chip	45

2.6.3 Heterogeneous Platform	45
2.6.4 Features of FPGA-SoC Heterogeneous Platform	
2.6.5 Memory Management on FPGA-SoC	
2.6.6 Quartus II Development Software	
2.6.7 Quartus Intellectual Property Libraries	
2.6.8 Linux Terminal Interface	
2.6.8.1 Linux Kernel Compilation	
2.7 Summary	
CHAPTER THREE: METHODOLOGY	
3.1 Overview	
3.2 Research Methodology	
3.3 Proposed Design Development and System Requirement	
3.3.1 Smart Water Quality System (SWQS)	
3.3.1.1 Interfacing Multiple Sensors	
3.4 SWQS Hardware Design	
3.5 SWQS Software Design	
3.6 Proposed Design Power Cycle	
3.7 Proposed Design Testing Plan	
3.8 The Design Cycle of The Proposed FPGA-Based SWQS	
3.8.1 The Hardware Design Flow of SWQS	70
3.8.1.1 Processors	
3.8.1.2 Memory	73
3.8.1.3 Clocking and Synchronization	73
3.8.1.4 Data Transfer Protocols	74
3.8.1.5 System Peripherals	75
3.8.1.6 Bridges	78
3.8.1.7 Pin Assignment	79
3.8.1.8 Synthesis Report	
3.8.2 The Software Design Flow of SWQS	
3.8.2.1 Firmware Development Flow	
3.8.2.2 The Linux Application Development Flow of	
SWQS	
3.9 The Embedded Linux Design Flow of SWQS	
3.9.1 Bootloader Compilation	
3.9.2 Root File-system Creation	
3.10 Adding New Core to SWQS Design	
3.11 Summary	
CHAPTER FOUR: RESULT AND ANALYSIS	89
4.1 Introduction	
4.2 Results	
4.2.1 The Results of the Quartus Project Compilation	
4.2.2 The Implementation of Prototype	
4.2.3 Design Verification Method	
4.2.4 The Results of the SWQS Linux-Based Application	
4.3 Discussion	
4.3 Discussion 4.3.1 Motivations of the Middleware Layer	
4.3.2 System Flexibility	
4.3.3 Applications of the Design	
+.3.3 Applications of the Design	

4.4 SWQS Design Compared to Previous Work	
4.5 Summary	
CHAPTER FIVE: CONCLUSION AND FUTURE WORK	
5.1 Conclusion	
5.2 Future Work	
REFERENCES	

LIST OF TABLES

Table 2.1	Summary Table	38
Table 2.2	Summary of All Sensors Used in Each Study Given in Table 2.1	43
Table 2.3	Files Generated After the Yocto Compilation	54

LIST OF FIGURES

Figure 1.1	Hardware Design Flow of FPGA (Intel, 2020)	3
Figure 2.1	Conventional-Based Water Quality Monitoring Example	
	(Tucsonaz, 2015)	10
Figure 2.2	IoT-Based Water Quality Monitoring Example Using Arduino	
	(Pinterest, 2017)	11
Figure 2.3	Configuration of pH Probe (Aaruththiran, Yujia, & Bagherian,	
	2019)	12
Figure 2.4	Configuration of Temperature Probe (Dhaker, 2020)	13
Figure 2.5	Turbidity Sensor	14
Figure 2.6	Electrical Conductivity Sensor	15
Figure 2.7	Dissolved Oxygen Optical Sensor (Staff, 2020)	15
Figure 2.8	Total Dissolved Solids Sensor	16
Figure 2.9	Free Chlorine Sensor (Karak et al., 2012).	17
Figure 2.10	Ultrasonic Level Sensor for Liquids	18
Figure 2.11	Overall Water Quality Monitoring System (Ngom et al., 2019)	19
Figure 2.12	Prototype of Water Quality Monitoring System (Li et al., 2018)	20
Figure 2.13	Overall Water Quality Scheme (Chowdury et al., 2019)	21
Figure 2.14	Overall System Architecture (Lezzar et al., 2020)	22
Figure 2.15	Hardware Implementation for Water Quality Monitoring Device	
	in Pipeline (Saravanan et al., 2018)	23
Figure 2.16	Experimental Setup of SQWM System (Mukta, Islam, Barman,	
	Reza, & Khan, 2019)	24
Figure 2.17	Circuit and Block Diagram of IoT System (Pujar et al., 2020)	25
Figure 2.18	System General Blocks and Data Flow (Encinas et al., 2017)	26
Figure 2.19	Block Diagram of Developed (Khatri et al., 2020)	27
Figure 2.20	IoT-based Monitoring System (Niswar et al., 2018)	28
Figure 2.21	System Architecture (Raju & Varma, 2017)	29
Figure 2.22	Overall Block Diagram (Vijayakumar & Ramya, 2015)	30
Figure 2.23	Overall Block Diagram (Geetha & Gouthami, 2016)	32
Figure 2.24	Overall Block Diagram (Billah et al., 2019)	33

Figure 2.25	The Block Diagram of Smart Water Quality Monitoring System	
	(Myint et al., 2017)	34
Figure 2.26	Block Diagram of Proposed System (Birje et al., 2016)	35
Figure 2.27	(a) Module 1: The Measurement and Sensing Module Block	
	Diagram (b) Module 2: The Notification Module Block	
	Diagram (Cloete et al., 2016)	36
Figure 2.28	Architecture of the E-Sensor AQUA System (Danh et al., 2020)	37
Figure 2.29	Cyclone V SoC FPGA from Intel (Intel PSG Website, 2020).	45
Figure 2.30	Example of a Memory Model of the Proposed SWQS Design	48
Figure 3.1	Research Methodology Phases	57
Figure 3.2	Research Methodology of the Proposed SWQS	58
Figure 3.3	Overall methodology of the Proposed SWQS	60
Figure 3.4	Proposed System Blocks and Data Flow	61
Figure 3.5	Multi-Core Heterogeneous System Architecture Design of the	
	Proposed Design	62
Figure 3.6	FPGA Single Core Processing Element of the Proposed Design	63
Figure 3.7	Proposed SWQS Hardware Proposed Data Acquisition Design	64
Figure 3.8	The Summary of the FPGA Hardware Design Flow	65
Figure 3.9	Firmware Applications for Each Core with SWQS Linux-based	
	Application	65
Figure 3.10	Flow Diagram of Firmware 0	66
Figure 3.11	The Sensor's Core Firmware Flow Diagram	67
Figure 3.12	The Proposed Design Abstraction Layers	68
Figure 3.13	The Architecture of the Proposed SWQS	71
Figure 3.14	The Configuration of the ARM Processor	72
Figure 3.15	Nios II Processor Configuration	72
Figure 3.16	The Configuration of On-chip-Memory Controller	73
Figure 3.17	Clock source IP in Platform Designer	73
Figure 3.18	PPL Configuration in Platform Designer	74
Figure 3.19	ADC Input Signals	75
Figure 3.20	System Timer IP Configurations in Platform Designer	75
Figure 3.21	mSGDMA Controller IP Configurations	76
Figure 3.22	Mutex configuration in Platform Designer	76
Figure 3.23	The Configuration of JTAG IP in Platform Designer	77

Figure 3.24	The Configuration of System ID Core in Platform Designer	77
Figure 3.25	Avalon Memory Mapped Controller IP	78
Figure 3.26	Address Span Extender IP	79
Figure 3.27	Top View of Pin Assignment	80
Figure 3.28	Synthesis Report of the Design	81
Figure 3.29	Nios II Software Development Flow	82
Figure 3.30	The Entire FPGA Development Flow	83
Figure 3.31	SWQS Application Memory Layout	84
Figure 3.32	FPGA Components Base Addresses	85
Figure 3.33	U-Boot Development Flow	87
Figure 3.34	Nios II Core Connections	87
Figure 4.1	The Result of the System Compilation	90
Figure 4.2	System Setup Components	90
Figure 4.3	Design Block Diagram	91
Figure 4.4	Core 1 pH Data Collection and Data Transfer Test Block	
	Diagram	93
Figure 4.5	Readings of pH Sensor	93
Figure 4.6	The Block Diagram of Core 2 TDS Data Collection and Data	
	Transfer Test	94
Figure 4.7	Readings of TDS Sensor	94
Figure 4.8	The Block Diagram of Core 3 Turbidity Data Collection and	
	Data Transfer Test	95
Figure 4.9	Readings of Turbidity Sensor	95
Figure 4.10	Line Graph of pH Values of Pure Water, Lemon Juice, and Milk	96
Figure 4.11	Testing the pH Sensor	96
Figure 4.12	Line graph of TDS Values of Pure Water and Water with Salt	97
Figure 4.13	Testing of the TDS Sensor	97
Figure 4.14	Line graph of Turbidity Values of Pure Water, Water with Little	
	Dust, and Water with More Dust	98
Figure 4.15	Testing the Turbidity Sensor	98
Figure 4.16	SWQS Results on Linux-Based Application	99
Figure 4.17	SWQS Proposed Single Design Core	101

CHAPTER ONE

INTRODUCTION

1.1 OVERVIEW

Water quality is an important factor that needs to be considered as it is directly related to people's lives. Therefore, this research focuses on designing a Smart Water Quality System (SWQS) Field Programmable Gate Array (FPGA)-based to eliminate the problems and drawbacks of previous works. This chapter illustrates the work by giving a brief background and defining the research problem. The chapter then presents the research motivation. Finally, it emphasizes the research scope.

Section 1.3 defines the research problem statement. Then, in Sections 1.4 and 1.5, the research objectives and research scope are presented, respectively. In addition, an outline of the main structure of the thesis is briefly reported in Section 1.6. Finally, Section 1.7 summarizes Chapter 1.

1.2 RESEARCH BACKGROUND

One of the major causes of death is consuming contaminated or polluted water. According to the World Health Organization (WHO), in 2017, 2.2 billion people were drinking water without any safety management services, and 144 million collected water from untreated water bodies, such as lakes, streams, and rivers ("2.1 Billion People Lack Safe Drinking Water at Home, More than Twice as Many Lack Safe Sanitation," 2017). To reduce the death rate due to contaminated and polluted water, measuring water quality, especially for consumption, becomes important. Water quality indicators can mean differently. It shows the suitability of any water body used for different uses, such as drinking, cooking, and cleaning. Water usage has different chemical, biological, and physical acceptance levels. For instance, drinking water has specified water quality parameters, such as pH levels ranging from 6.5 to 8.5. As many parameters need to be measured, thus, several sensors must be employed for the water quality test. To this date, the water safety management services that utilize a system that support large computational loads need a huge amount of power, not portable, and big devices, making it impossible to be commercialized.

Hence, it is pertinent to establish a new smart system considering the latest technological advancement that can carry out the huge computational load at lower power but with high performance. Therefore, this research proposes a water quality system that utilizes the FPGA platform and the Adcanced RISC Machine (ARM) processor.

1.2.1 Field Programmable Gate Array (FPGA)

FPGA is a reconfigurable computing device with several programmable units that could solve any computational issues (Giesemann, Paya-Vaya, Blume, Limmer, & Ritter, 2014). This device is an integrated circuit made of semiconductor material, and the main feature of FPGA is the device's electrical functionality can be reconfigured even by the customer. As a result, these powerful devices can be customized to accelerate key workloads and enable design engineers to adapt to emerging standards or changing requirements.

Figure 1.1 illustrates the common design flow for an FPGA platform, beginning with hardware design specifications. The hardware design specifications consist of the needed hardware design's functionality, memory size, the number of input/output ports, speed, and finally, how the data transfers. The next step is the architecture design, in which the hardware design can be further split into system and sub-system modules, i.e., the micro-architecture level design (Gerstlauer et al., 2009).

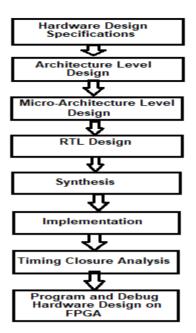


Figure 1.1 Hardware Design Flow of FPGA (Intel, 2020)

Once the architecture and the micro-architecture level of the needed hardware design are completed, the Register Transfer Level (RTL) will begin. At this level, Hardware Description Language (HDL) will be used to translate the system and subsystem blocks into a Hardware netlist ("AN 311: Standard Cell ASIC to FPGA Design Methodology and Guidelines," 2009). Synthesis and implementation processes will begin when the digital module design is done. These two steps will translate the HDL design into a physical netlist prepared for timing analysis. Timing analysis is the process of ensuring the hardware design is working from a time perspective. In other words, it will check whether the design is the speed requirements of the system or not (Gerstlauer et al., 2009). In the end, the hardware design will be executed on an FPGA board.

1.2.2 Heterogeneous System Architecture (HSA)

A Heterogeneous System Architecture (HSA) is a computer platform that functions with associated software that makes different kinds of processors with different architectures work in shared memory efficiently and cooperatively from a single source program (Kyriazis, 2012). Integrating multiple computing elements at low frequencies leads to high performance with low power consumption; architectural heterogeneity improves platform flexibility (Burgio et al., 2016). This heterogeneous platform, such as FPGA-System-on-Chip (SoC), improves the performance of embedded using

hardware containing more than one type of processor. This approach has shown improved performance, particularly in artificial intelligence (AI), in which computationally demanding models must be trained and executed.

SWQS utilizes different sensors to measure water parameters such as pH, turbidity, and Total Dissolved Solids (TDS) and then processes the data on FPGA-SoC. The proposed design methodology reduces the complexity of the FPGA-SoC heterogeneous platform by adding a middleware layer for software developers to interact with the FPGA system in the form of an application program interface. Therefore, heterogeneous architecture is the best choice for complex systems with multiple input and output ports to enhance the overall system performance.

1.3 PROBLEM STATEMENT

Currently, in Malaysia, water quality monitoring is done by traditional methods, consisting of taking samples from the area under test and then driving them back to a laboratory to analyze them. The analysis usually is for detecting chemicals and microbial that cause the water's pollution. This method is not only time-consuming but requires significant human interaction. As a result, important data may be lost because of the manual collection process. In addition, the water quality analysis is not done within a short time, so determining a real-time water condition is not plausible. This traditional method is only good if the samples are taken and analyzed simultaneously (Geetha & Gouthami, 2016). Moreover, the water might get contaminated, making it very difficult and costly to recover (Billah, Yusof, Kadir, Ali, & Ahmad, 2019). Moreover, the technicians cannot take samples from all locations, which may lead to inaccurate data (Lezzar, Benmerzoug, & Kitouni, 2020). Besides the issues arising from the manual sample collection, the chemical materials used in water quality testing are usually toxic and very expensive (Khatri, Gupta, & Gupta, 2020).

Even though the research on water quality monitoring systems have been applied many times, the current system is still expensive, has short-distance data transmission, and is not easy to use (Geetha & Gouthami, 2016). Most current SWQS is costly (Pasika & Gandla, 2020), and there should be a big effort by researchers to reduce the cost to make the system more affordable for everyone. Performance is also an important issue

that needs to be considered. SWQS must have high performance and accuracy to reduce errors that might cause poor health conditions and death for the people who consumed the water if the measurements are incorrect.

While FPGA has high processing power, developing an FPGA can be complex and requires more effort than configuring the same design on the Central Processing Unit (CPU) (Besta, Stanojevic, Licht, Ben-Nun, & Hoefler, 2019). In addition, it provides less specialized components (i.e., floating point) operations. It is for this reason that FPGA remains to be a prototype platform for embedded systems. That said, the use of heterogeneous platforms mesh with FPGA has recently gained popularity for design applications that need performance and programmability offered via a processor and flexibility and configurability accomplished using the FPGA fabric (Zhong, Niar, Prakash, & Mitra, 2016). The SoC heterogeneous platforms improve the performance of embedded systems using a hardware design that contains more than one processor.

In addition, when comparing FPGA with other processors such as Arduino and Raspberry Pi, in terms of configurability and implementation, FPGA is reconfigurable based on the user's requirements. However, Arduino and Raspberry Pi are configured and implemented during manufacturing. Additionally, FPGA can process the data in parallel to overcome the latency issue when many inputs are used. On the other hand, there is no way to perform pipelines using processors such as Arduino and Raspberry Pi. In addition, the processing rate of the SWQ data using an FPGA processor is high as its frequency reaches 1 GHz. However, the frequency is slightly lower in other processors, for instance, 16 MHz and 400 MHz for Arduino and Raspberry Pi, respectively. Last but not least, the pins of FPGA are 40 pins that are not hardcoded as their interface can be modified based on the sensor's data exchange protocol, unlike the pins of Arduino and Raspberry Pi, which are hardcoded during the manufacturing process. Moreover, FPGA-SoC is a heterogeneous platform that can work with shared memory for more cooperativity and efficiency. In addition, a heterogeneous platform such as FPGA-SoC improves the performance of embedded using more than one processor.

For these reasons, the main objective of this project is to design SWQS using an FPGA-SoC platform to monitor different water parameters, namely; pH, TDS, and turbidity parameters, rather than relying on the conventional way of measuring water quality parameters.

1.4 RESEARCH OBJECTIVES

The main objectives of the project are as below:

- To design a reconfigurable hardware-based Smart Water Quality System (SWQS) via using a Field Programmable Gate Array-System-on-Chip (FPGA-SoC) heterogeneous platform.
- To implement a real-time prototype for the proposed Smart Water Quality System (SWQS).
- iii. To evaluate the proposed Smart Water Quality System (SWQS) based on pH, Total Dissolved Solids (TDS), and turbidity parameters.

1.5 RESEARCH SCOPE

The scope of this research mainly concentrates only on the hardware design of SWQS by utilizing the heterogeneous platform of FPGA-SoC to process signals obtained from water quality sensors. The system design integrates FPGA with the SoC to create a customizable heterogeneous platform that segments the system functionality into tasks. The proposed design in this study will utilize two development kits, the DE10 Nano FPGA-SoC development kit from Intel and the Raspberry Pi development board. The utilized boards will not impact the proposed system design since the design flow is the same for any FPGA development board. The system has two SoC sub-systems: an external one (Raspberry Pi) and an internal one (ARM SoC). The external sub-system will provide the system with all the required augments to ease prototype implementation, like LCD, mouse, and keyboard. The internal SoC will be part of the SWQS as the main system processor.

In addition, testing the proposed system will only be based on three water quality parameters to verify and validate the functionality and reliability of the proposed FPGA-SoC platforms. The utilized sensors in this design will be the pH, TDS, and turbidity sensors. These sensors were used as a proof-of-concept to validate the system's functionality. However, other sensors related to SWQS can be adapted to any future system based on the user's requirements.

1.6 DISSERTATION LAYOUT

This dissertation is composed of five chapters; a brief introduction and overview of the research are provided in Chapter 1. In Chapter 2, an in-depth investigation was conducted about the previous studies in the SWQS development field. Chapter 3 elaborates on the proposed system, and the design steps needed to develop an SWQS hardware design based on a heterogeneous platform are presented as well as presenting the flow of software to program the system. Furthermore, the proposed system test results and the collected data, were discussed in Chapter 4. Finally, in Chapter 5, the summary of the research findings, contribution, claims, and comparative analysis was reported.

1.7 SUMMARY

This chapter presented a detailed overview of the research topic, known as SWQS. First, the problem statement of this study was illustrated. Then, the research objectives are presented in this chapter. Furthermore, the scope was explained. Finally, the thesis layout and the relation between each chapter were discussed.

CHAPTER TWO

LITERATURE REVIEW

2.1 OVERVIEW

This chapter describes the academic literature correlated with Smart Water Quality System (SWQS) hardware implementation. The main objective of this chapter is to find out and elaborate on the latest research achievements in the field of SWQS design and development. In addition, this chapter highlighted the drawbacks and problems encountered by researchers in their designs, as well as obstacles in providing suitable SWQS solutions.

In Section 2.2, a brief overview of water quality approaches is presented. Then, Section 2.3 explains some sensors that measure water quality parameters such as pH, temperature, turbidity, electrical conductivity (EC), and dissolved oxygen (DO). In Section 2.4, previous studies have been presented based on the controller or the processor. They have been used to collect data on water quality parameters and summarize the related studies' motivations and drawbacks. Section 2.5, on the other hand, shows the proposed SWQS FGPA-based followed by Section 2.6. It presents general information about FPGA in terms of architecture, such as memory, speed, interfaces, etc., and software tools, such as Quartus, Platform Designer, etc. Finally, Section 2.7 summarizes this chapter.

2.2 DIFFERENT WATER QUALITY APPROACHES

There are two ways of measuring water quality. The first is the traditional method involving samples from the river, lake, or any water source, while the second uses sensors to measure water quality. In the following subsections, both conventional and Internet of Things (IoT) methods will be discussed in detail.

2.2.1 Conventional Approach

The traditional way of measuring water quality parameters, such as the water pH, turbidity, DO, and EC, starts with several samples for testing. Note that sampling selects a small portion of the water to be handled and transported to the laboratory (Ngom, Diallo, Gueye, & Marilleau, 2019). After transporting the samples to the laboratory, specific materials or solutions must be added to measure a specific parameter. For example, to measure the level of phosphorus, one of the crucial water parameters, samples must be transferred to the lab as soon as possible to minimize any external effects that might change the measurement of the total phosphorus. Potassium persulfate should be mixed with the water sample before heating it for 30 minutes. After the heating process, the mixture must be cooled to room temperature. Before measuring the total phosphorus, sodium hydroxide is added and mixed with the sample gently. The last step is to measure the total phosphorus using a spectrophotometer device 7 minutes after mixing. Sometimes, the process can take more than five working days (Li, Jaafar, & Ramli, 2018).

Besides the elaborated identification process, the sampling process is not easy as the samples must be taken from the specified location and involve a highly complex process. Additionally, water samples should be transferred to the laboratory and tested as soon as possible to avoid water pollution. Moreover, this method is time-consuming and costly, requiring equipment cleaning, measuring procedures, and recording. Finally, due to human interaction, many errors might occur during the process, and that will affect the accuracy of the reading.

To conclude, this method is inefficient, and more research should be conducted to develop alternative methods to avoid the challenges mentioned above. Figure 2.1 shows an example of measuring water quality using the traditional method.