SHIFTED COMPLETELY CONNECTED NETWORK (SCCN): ARCHITECTURE OF HIERARCHICAL INTERCONNECTION NETWORK TO IMPROVE THE PERFORMANCE OF MASSIVELY PARALLEL COMPUTER SYSTEMS

BY

MOHAMMED N. M. ALI

A thesis submitted in fulfilment of the requirement for the degree of Doctor of Philosophy in Computer Science

Kulliyyah of Information and Communication Technology
International Islamic University Malaysia

February 2020

ABSTRACT

At the current time, finding an alternative computing device with extreme computation power became the main concern of the research community. Therefore, building a computer device able to execute extremely difficult calculations in a short time is required. Presently, massively parallel computer (MPC) systems considered the highest computing devices, and the existence of these systems is important to execute many operations in many sectors such as engineering and science. These systems built based on an internal network called interconnection network which has a particular design represented by the network topology. The performance of these networks affected widely by the network topology. Besides, the cost of these networks influenced by the price of the processing elements (PEs) and the communication links. Thus, the design of the interconnection network topology has a crucial impact on the network cost and performance. Many topologies of interconnection networks have been presented to be used as basic modules in building MPC systems. However, the earlier topologies showed a lack of performance in case of increasing the size of the interconnection network. As a result, hierarchical interconnection networks (HINs) proposed to replace these networks. Currently, many HINs introduced to enhance the performance of MPC systems, however, we still lack a good one. In this research, a hierarchical interconnection network proposed as a basic module (BM) to build a complete parallel computer system. This topology is a completely connected network composed of six nodes and called shifted completely connected network (SCCN), also, it connected hierarchically to produce higher-levels leading to a complete system network. A two-dimensional system with multiple levels is built based on SCCN. The two-dimensional levels which composing this system are network-on-chip level, board-level, cabinet-level, and system-level. The static network performance parameters of these levels evaluated by computer simulators and the obtained results compared to multiple conventional and hierarchical interconnection networks. Moreover, in this research, we presented a three-dimensional design of SCCN based on the proposed topology. Therefore, a three-dimensional network-on-chip (3D-NoC) presented to build higher levels of 3D-SCCN. The static network performance parameters of 3D-NoC level and the higher levels assessed by computer simulators. Furthermore, the obtained results compared to other conventional and hierarchical interconnection networks. The purpose of the comparison is to prove the strength of the proposed topology which showed promising results in many aspects.

خلاصة البحث

في الوقت الحالي ايجاد جهاز كمبيوتر بديل ذو كفاءة عالية أصبح من أكثر إهتمامات الباحثين. لذلك بناء جهاز كمبيوتر قادر على تنفيذ اعداد كبيرة من الحسابات الصعبة في فترات زمنية قصيرة أصبح أمرا ملحاً. في وقتنا الحالي أنظمة الكمبيوتر المتوازية تعتبر أقوى أجهزة كمبيوتر في العالم , حيث أن وجود هذه الأجهزة هو شيء ضروري لإنجاز كثير من العمليات الحسابية في جميع المجالات وخصوصا في مجالي الهندسة والعلوم . هذه الأجهزة تم بناؤها بإستخدام شبكات تسمى الشبكات الداخلية والتي لها تصاميم محددة متمثلة في طوبولوجيا الشبكة . طبولوجيا الشبكة لها تأثير كبير على أداء هذه الشبكات وكذلك أسعار بناء هذه الشبكات مرتبط ارتباطاً وثيقاً بسعر عناصر المعالجة وأسلاك التوصيل. نستنتج من ذلك بأن تصميم الطوبولوجيا لهذه الشبكات له تأثير حقيقي على أداء وسعر تركيب هذه الشبكات . العديد من المخططات (الطوبولوجيا) للشبكات الداخلية قد تم تقديمها لتستخدم كوحدات أساسية في بناء أجهزة الكمبيوتر المتوازية ولكن الشبكات التي قدمت في الفترات الأولى أظهرت قصوراً في الأداء خصوصاً في حالة زيادة حجم الشبكات الداخلية . لذلك تم تقديم الشبكات الداخلية الهرمية لتكون بديلاً عنها في بناء أجهزة الكمبيوتر المتوازية . حاليا هناك عدد كبير من الشبكات الداخلية الهرمية قد تم تقديمها ولكن لم تثبت أي شبكة منها تفوقها على الشبكات الأخرى حتى الان . في هذا البحث شبكة داخلية هرمية جديدة قد تم تقديمها من أجل استخدامها في بناء أجهزة الكمبيوتر المتوازية . هذه الشبكة هي عبارة عن شبكة متصلة كليا ومتكونة من ستة عقد ولقد تم تسميتها شبكة الإزاحة المتصلة كليا. هذه الشبكة قد تم تقديمها لتستخدم كوحدة أساسية في بناء هذه الأجهزة الضخمة . لذلك في هذا البحث تم توصيل هذه الشبكة بصورة هرمية لإنتاج مستويات من شبكات أعلى وأكبر حجماً. وأيضاً في هذا البحث قمنا بتقديم نظام ثنائي الأبعاد , هذا النظام مبني من مجموعة مستويات قد تم انشاؤها بناءاً على شبكة الإزاحة المتصلة كلياً والتي تم تقديمها في هذا البحث . المستويات ثنائية الأبعاد التي تم تقديمها في هذا البحث تتكون من مستوى شبكة الرقاقة ,المستوى اللوحي , مستوى الخزانة , مستوى النظام الكامل. عوامل أداء الشبكة الثابتة لهذه المستويات قد تم تقييمها في هذا البحث بأستخدام محاكيات الكمبيوتر والنتائج التى تم الحصول عليها تم مقارنتها مع عدد كبير من الشبكات التقليدية والشبكات الهرمية الداخلية. أيضا في هذا البحث قمنا بتقديم التركيب ثلاثي الأبعاد من شبكة الإزاحة المتصلة كلياً. لذلك شبكة الرقاقة الثلاثية قد تم تقديمها و تم استخدامها في بناء مستويات أعلى بأعداد أكبر من العقد. أيضا عوامل أداء الشبكة الثابتة للمستويات ثلاثية الأبعاد قد تم تقييمها باستخدام محاكيات الكمبيوتر والنتائج التى تم الحصول عليها تم مقارنتها مع عدد كبير من الشبكات التقليدية والهرمية. الهدف من عملية المقارنة هو اظهار كفاءة وقوة الشبكة المقدمة من خلال هذا البحث والتى أعطت نتائج جيدة جداً في أكثر من جانب.

APPROVAL PAGE

The thesis of Mohammed N. M. Ali has been approved by the following:

_____
Adamu Abubakar Ibrahim
Supervisor

_____
M.M. Hafizur Rahman
Co-Supervisor

_____
Rizal Mohd Nor
Internal Examiner

_____
Ravie Chandran Muniyandi
External Examiner

_____
Mohamed Taher Ben Othman
External Examiner

_____
Amir Akramin bin Shafie
Chairman

DECLARATION

I hereby declare that this thesis is the result of my own investigations, except where otherwise stated. I also declare that it has not been previously or concurrently submitted as a whole for any other degrees at IIUM or other institutions.

Mohammed N. M. Ali

Signature ..... Date .....

INTERNATIONAL ISLAMIC UNIVERSITY MALAYSIA

DECLARATION OF COPYRIGHT AND AFFIRMATION OF FAIR USE OF UNPUBLISHED RESEARCH

SHIFTED COMPLETELY CONNECTED NETWORK (SCCN): ARCHITECTURE OF HIERARCHICAL INTERCONNECTION NETWORK TO IMPROVE THE PERFORMANCE OF MASSIVELY PARALLEL COMPUTER SYSTEMS

I declare that the copyright holders of this thesis are jointly owned by the student and IIUM.

By signing this form, I acknowledged that I have read and understand the IIUM Intellectual Property Right and Commercialization policy.
Affirmed by Mohammed N. M. Ali

……..…….. ……..
Signature Date

ACKNOWLEDGEMENTS

Firstly, it is my utmost pleasure to dedicate this work to my dear parents and my family, who granted me the gift of their unwavering belief in my ability to accomplish this goal: thank you for your support and patience.

I wish to express my appreciation and thanks to those who provided their time, effort and support for this project. To the members of my dissertation committee, thank you for sticking with me.

Finally, a special thanks to my supervisor Dr. Adamu Abubakar Ibrahim, and my co-supervisor Dr. M.M. Hafizur Rahman for their continuous support, encouragement and leadership, and for that, I will be forever grateful.

TABLE OF CONTENTS

Abstract ii
Abstract in Arabic iii
Approval Page iv
Declaration v
Copyright Page vi
Acknowledgements vii
List of Tables xiv
List of Figures xv
List of Abbreviations xx

CHAPTER ONE: INTRODUCTION 1
1.1 Background of the Study 1
1.2 Statement of the Problem 4
1.3 Research Objectives 5
1.4 Methodology 6
1.5 Research Questions 6
1.6 Scope of The Study 7
1.7 Significance of the Study 7
1.8 Chapter Summary 8

CHAPTER TWO: LITERATURE REVIEW 10
2.1 Introduction 10
2.2 Conventional Interconnection Networks 12
2.2.1 Completely Connected Network 13
2.2.2 Linear Array Topology 13
2.2.3 Ring Topology 14
2.2.4 Star Topology 15
2.2.5 Tree Network 16
2.2.6 Fat-Tree Topology 16
2.2.7 Hypercube Topology 18
2.2.8 K-ary n-cube Network 19
2.2.9 Two Dimensional Mesh (2D-Mesh) Network 20
2.2.10 Two Dimensional Torus (2D-Torus) Network 21
2.3 Hierarchical Interconnection Networks (HIN) 22
2.3.1 Tori Connected Mesh (TESH) 22
2.3.2 Tori Connected Torus Network (TTN) 25
2.3.3 Hierarchical Torus Network (HTN) 27
2.3.4 Dragonfly Network 30
2.3.5 Triplet Network 33
2.3.6 Block Shifted Network 35
2.3.7 Cube Connected Cycle Network 37
2.3.8 Symmetric Tori Connected Torus Network (STTN) 38
2.4 Three Dimensional (3D) Interconnection Networks 39
2.4.1 Three Dimensional Mesh Network (3D-Mesh) 40

2.4.2 Three Dimensional Torus Network (3D-Torus) 41
2.4.3 Hierarchical 3D-Mesh Network (H3DM) 43
2.4.4 Hierarchical 3D-Torus Network (H3DT) 45
2.4.5 Modified Hierarchical 3D-Torus Network (MH3DT) 46
2.4.6 Hierarchical 3D-TESH Network (3D-TESH) 49
2.4.7 Hierarchical Tori Connected Mesh (HTM) Network 51
2.5 Supercomputers 51
2.5.1 Tianhe-2 (MilkyWay-2) Supercomputer 52
2.5.2 Sunway TaihuLight Supercomputer 54
2.6 Gaps In The Literature 57
2.7 Chapter Summary 59

CHAPTER THREE: 2D-Shifted Completely Connected Network (2D-SCCN) Architercture 60
3.1 Introduction 60
3.2 The Basic Module (BM) of SCCN 62
3.3 The Network-on-Chip Level of SCCN 65
3.3.1 Node Addressing of NoC Level of SCCN 73
3.3.2 Routing Algorithm of the NoC Level of SCCN 75
3.4 The Board Level (Level-3) of SCCN 80
3.4.1 Node Addressing of Level-3 of SCCN 88
3.4.2 Routing Algorithm of Level-3 of SCCN 90
3.5 The Cabinet Level (Level-4) of SCCN 97
3.5.1 Nodes Addressing of Level-4 of SCCN 105
3.5.2 Routing Algorithm of Level-4 of SCCN 108
3.6 The System Level (Level-5) of SCCN 118
3.6.1 Node Addressing of Level-5 Network 128
3.6.2 Routing Algorithm of Level-5 Network 132
3.7 Chapter Summary 143

CHAPTER FOUR: EXPERIMENTAL ANALYSIS AND PRESENTATION OF RESULTS 144
4.1 Introduction 144
4.2 Static Network Performance For Level-1 Network of SCCN (The Proposed Topology Level) 148
4.2.1 Node Degree of the Basic-Module Level 149
4.2.2 Network Diameter of the Basic-Module Level 150
4.2.3 Cost of the Basic-Module Level 152
4.2.4 Average Distance of the Basic-Module Level 152
4.2.5 Arc Connectivity of the Basic-Module Level 153
4.2.6 Bisection Width (BW) of the Basic-Module Level 154
4.2.7 Wiring Complexity of the Basic-Module Level 154
4.2.8 Packing Density of the Basic-Module Level 155
4.2.9 Message Traffic Density of the Basic-Module Level 156
4.2.10 Cost Effective Factor (CEF) of the Basic-Module Level 157
4.2.11 Time-Cost Effectiveness Factor (TCEF) of the Basic-Module Level 161
4.2.12 Static Cost Effective Analysis of the Basic-Module Level 163
4.2.13 Fault Tolerance of the Basic-Module Level 165

4.2.14 Fault Diameter of the Basic-Module Level....166
4.3 Static Network Performance For Level-2 Network of SCCN (The NoC Level)....167
4.3.1 Node Degree of the NoC-Level....169
4.3.2 Diameter of the NoC-Level....169
4.3.3 Cost of the NoC-Level....170
4.3.4 Average Distance of the NoC- Level....171
4.3.5 Arc Connectivity of the NoC- Level....172
4.3.6 Bisection Width (BW) of the NoC-Level....172
4.3.7 Wiring Complexity (WC) of the NoC-Level....173
4.3.8 Packing Density of the NoC-Level....175
4.3.9 Message Traffic Density of the NoC-Level....176
4.3.10 Cost Effectiveness Factor (CEF) of the NoC-Level....177
4.3.11 Time-Cost Effectiveness Factor (TCEF) of the NoC-Level....178
4.3.12 Static Cost Effective Analysis of the NoC-Level....180
4.3.13 Fault Tolerance of the NoC-Level....183
4.3.14 Fault Diameter of the NoC-Level....185
4.4 Static Network Performance For Level-3 Network of SCCN (The Board Level)....187
4.4.1 Node Degree of the Board-Level....189
4.4.2 Diameter of the Board-Level....191
4.4.3 Average Distance of the Board-Level....194
4.4.4 Cost of the Board- Level....196
4.4.5 Arc Connectivity of the Board- Level....197
4.4.6 Bisection Width (BW) of the Board-Level....198
4.4.7 Wiring Complexity (WC) of the Board-Level....200
4.4.8 Packing Density of the Board-Level....203
4.4.9 Message Traffic Density of the Board-Level....205
4.4.10 Cost Effectiveness Factor (CEF) of the Board-Level....206
4.4.11 Time-Cost Effectiveness Factor (TCEF) of the Board-Level....208
4.4.12 Static Cost Effective Analysis of the Board-Level....210
4.4.13 Fault Tolerance of the Board-Level....213
4.4.14 Fault Diameter of the Board-Level....214
4.4.15 Static Network Performance Parameters of (8×8) Level-3 Network of SCCN....217
4.4.16 Some Generalization....218
4.5 Static Network Performance For Level-4 Network of SCCN (The Cabinet Level)....220
4.5.1 Node Degree of the Cabinet-Level....221
4.5.2 Diameter of the Cabinet-Level....223
4.5.3 Average Distance of the Cabinet-Level....225
4.5.4 Cost of the Cabinet- Level....227
4.5.5 Arc Connectivity of the Cabinet- Level....228
4.5.6 Bisection Width (BW) of the Cabinet-Level....229
4.5.7 Wiring Complexity (WC) of the Cabinet-Level....230
4.5.8 Packing Density of the Cabinet-Level....233
4.5.9 Message Traffic Density of the Cabinet-Level....235
4.5.10 Cost Effectiveness Factor (CEF) of the Cabinet-Level....236
4.5.11 Time-Cost Effectiveness Factor (TCEF) of the Cabinet-Level....238

4.5.12 Static Cost Effective Analysis of the Cabinet-Level 240
4.5.13 Fault Tolerance of the Cabinet-Level 243
4.5.14 Fault Diameter of the Cabinet-Level 244
4.5.15 Some Generalization 246
4.6 Static Network Performance For Level-5 Network of SCCN (The System-Level) 248
4.6.1 Node Degree of the System-Level 249
4.6.2 Diameter of the System-Level 251
4.6.3 Average Distance of the System-Level 254
4.6.4 Cost of the System- Level 255
4.6.5 Arc Connectivity of the System- Level 257
4.6.6 Bisection Width (BW) of the System-Level 259
4.6.7 Wiring Complexity (WC) of the System-Level 260
4.6.8 Packing Density of the System-Level 264
4.6.9 Message Traffic Density of the System-Level 266
4.6.10 Cost Effectiveness Factor (CEF) of the System-Level 268
4.6.11 Time-Cost Effectiveness Factor (TCEF) of the System-Level ... 270
4.6.12 Static Cost Effective Analysis of the System-Level 272
4.6.13 Fault Tolerance of the System-Level 276
4.6.14 Fault Diameter of the System-Level 278
4.6.15 Scalability of SCCN 281
4.6.15 Some Generalization 282
4.7 Chapter Summury 284

CHAPTER FIVE: ARCHITECTURE OF 3D-SHIFTED COMPLETELY CONNECTED NETWORK (3D-SCCN) 286
5.1 Introduction 286
5.2 Architecture of the Basic Module (BM) of the 3D-SCCN (Level-0 Network) 289
5.3 Architecture of the 3D Network-on-Chip Level (3D-NoC) of SCCN .. 291
5.3.1 Node Addressing 298
5.3.2 Routing Algorithm for the 3D-NoC Level of SCCN 300
5.4 The Architecture of the Level-2 of the 3D-SCCN 310
5.4.1 Node Addressing of the Level-2 Network of the 3D-SCCN 319
5.4.2 Routing Algorithm for the Level-2 Network of the 3D- SCCN ... 323
5.5 Structural Design of Level-3 of the 3D-SCCN 335
5.5.1 The Basic Module (BM) of the Level-3 of the 3D-SCCN 336
5.5.2 The Structure of the Level-3 of the 3D-SCCN Network 339
5.5.3 Node Addressing of the Level-3 Network of the 3D-SCCN 346
5.5.4 Routing Algorithm for the Level-3 Network of the 3D- SCCN ... 349
5.6 Chapter Summury 364

CHAPTER SIX: THE PERFORMANCE AND THE EVALUATION OF THE 3D-SCCN NETWORK 365
6.1 Introduction 365
6.2 The Evaluation of the 3D-NoC Level of SCCN 366
6.2.1 Node Degree of the 3D-NoC Level of SCCN 367
6.2.2 Diameter of the 3D-NoC Level of SCCN 368
6.2.3 Cost of the 3D-NoC Level of SCCN 369

6.2.4 Average Distance of the 3D-NoC Level of SCCN 369
6.2.5 Arc Connectivity of the 3D-NoC Level of SCCN 370
6.2.6 Bisection Width (BW) of the 3D-NoC Level of SCCN.....371
6.2.7 Wiring Complexity of the 3D-NoC Level of SCCN.....371
6.2.8 Packing Density of the 3D-NoC Level of SCCN 374
6.2.9 Message Traffic Density of the 3D-NoC Level of SCCN 375
6.2.10 Cost Effective Factor (CEF) of the 3D-NoC Level of SCCN.....376
6.2.11 Time-Cost Effectiveness Factor (TCEF) of 3D-NoC Level of SCCN.....378
6.2.12 Static Cost Effective Analysis of the 3D-NoC Level of SCCN.....379
6.2.13 Fault Tolerance of the 3D-NoC Level of SCCN.....382
6.2.14 Fault Diameter of the 3D-NoC Level of SCCN.....383
6.3 The Static Network Performance Parameters of Level-2 of the 3D-SCCN.....385
6.3.1 Node Degree of Level-2 of the 3D-SCCN.....386
6.3.2 Diameter of Level-2 of the 3D-SCCN 388
6.3.3 Cost of Level-2 of the 3D-SCCN.....389
6.3.4 Average Distance of Level-2 of the 3D-SCCN 390
6.3.5 Arc Connectivity of Level-2 of the 3D-SCCN 391
6.3.6 Bisection Width (BW) of Level-2 of the 3D- SCCN.....392
6.3.7 Wiring Complexity of Level-2 of the 3D-SCCN.....393
6.3.8 Packing Density of Level-2 of the 3D-SCCN.....396
6.3.9 Message Traffic Density of Level-2 of the 3D-SCCN 397
6.3.10 Cost Effective Factor (CEF) of Level-2 of the 3D-SCCN.....398
6.3.11 Time-Cost Effectiveness Factor (TCEF) of Level-2 of 3D-SCCN.....400
6.3.12 Static Cost Effective Analysis of Level-2 of the 3D-SCCN.....401
6.3.13 Fault Tolerance of Level-2 of the 3D-SCCN.....403
6.3.14 Fault Diameter of Level-2 of the 3D-SCCN.....405
6.4 Static Network Performance Parameters of Level-3 of the 3D-SCCN ..409
6.4.1 Node Degree of Level-3 of the 3D-SCCN.....410
6.4.2 Diameter of Level-3 of the 3D-SCCN 411
6.4.3 Cost of Level-3 of the 3D-SCCN.....413
6.4.4 Average Distance of Level-3 of the 3D-SCCN 414
6.4.5 Arc Connectivity of Level-3 of the 3D-SCCN 415
6.4.6 Bisection Width (BW) of Level-3 of the 3D- SCCN.....417
6.4.7 Wiring Complexity of Level-3 of the 3D-SCCN.....419
6.4.8 Packing Density of Level-3 of the 3D-SCCN.....422
6.4.9 Message Traffic Density of Level-3 of the 3D-SCCN 423
6.4.10 Cost Effective Factor (CEF) of Level-3 of the 3D-SCCN.....425
6.4.11 Time-Cost Effectiveness Factor (TCEF) of Level-3 of 3D-SCCN.....426
6.4.12 Static Cost Effective Analysis of Level-3 of the 3D-SCCN.....429
6.4.13 Fault Tolerance of Level-3 of the 3D-SCCN.....432
6.4.14 Fault Diameter of Level-3 of the 3D-SCCN.....433
6.4.15 Tables of the Comparison between Level-3 of SCCN and other Networks 438
6.5 Chapter Summury 439

CHAPTER SEVEN: CONCLUSIONS AND FUTURE WORK 441
7.1 Introduction 441
7.2 Conclusions 442
7.3 Future Work 447

REFERENCES 448

APPENDIX A: FLOW CHART OF THE PROPOSED WORK 459
APPENDIX B: ROUTING ALGORITHM BETWEEN TWO NODES IN LEVEL-3 OF SCCN 460
APPENDIX C: ROUTING DECISION BETWEEN TWO NODES IN LEVEL-4 NETWORK OF SCCN 461
APPENDIX D: ROUTING DECISION BETWEEN TWO NODES IN LEVEL-5 NETWORK OF SCCN 463

PUBLICATIONS 465

LIST OF TABLES

Table No.		Page No.
3.1	A collection of interconnection network topologies used in commercial and experimental parallel computers	61
4.1	The static network performance parameter of Level-1 Network of SCCN	150
4.2	Comparison between Level-2 SCCN and other networks	175
4.3	Comparison between Level-2 and other networks	184
4.4	Comparison of Static Network Performance Parameters of Various Networks	203
4.5	Comparison of Static Network Performance Parameters of Various Networks	211
4.6	Comparison between (4×4) and (8×8) Level-3 of SCCN	217
4.7	Comparison of the static performance parameters of SCCN and various networks	234
4.8	Static Network Parameters Comparison of Various Interconnection Networks	239
4.9	Total Number of Nodes of Various Networks in Different Levels	249
6.1	Comparison between 3D-NoC and Various Networks	374
6.2	Static Network Performance Comparison of 3D-NoC and Various Networks	381
6.3	Static Network Performance Parameters Comparison of Level-2 of 3D-SCCN and Different Networks	395
6.4	Static performance Parameters Comparison between Level-2 of the 3D-SCCN and Various Networks	404
6.5	Static Network Performance Comparison of Level-3 of the 3D-SCCN and Different Networks	438
6.6	Static Network Performance Comparison of Level-3 of the 3D-SCCN and Different Networks	439

LIST OF FIGURES

Figure No.		Page No.
2.1	Completely Connected Network	14
2.2	Linear Array Topology	14
2.3	Ring Topology	15
2.4	Star Topology	15
2.5	Tree Topology	16
2.6	Fat-Tree Topology	17
2.7	Hypercube Network	18
2.8	Different k-ary n-cube Networks	19
2.9	Mesh Topology	20
2.10	Torus and Folded Torus Networks	21
2.11	Level_1 of TESH Network	24
2.12	Level_2 of TESH Network	24
2.13	Interconnection of TTN (a) Basic Module (b) Higher Level Network	27
2.14	Basic Module of HTN	30
2.15	Level-2 of HTN	30
2.16	(a) Block diagram of a group (virtual router) (b) high-level block diagram of dragonfly topology composed of multiple groups	33
2.17	The topolgy of THIN (a) Level-0 THIN; (b) Level-1 THIN; (c) Level-2 THIN; (d) Level-3 THIN	34
2.18	A BSN (2, 2) with N = 16	37
2.19	A BSN (1, 2) with N = 16	37
2.20	Cube-Connected-Cycles of 24 Nodes	38
2.21	Interconnection of STTN (Basic Module and Higher Level)	39
2.22	3D-Mesh Network	41

2.23	3D-Torus Network	43
2.24	Basic Module of H3DM	44
2.25	Level-2 of H3DM	45
2.26	Interconnection of Level-2 Network of H3DT	46
2.27	BM of MH3DT Network	47
2.28	Level-2 of MH3DT	48
2.29	$(4 \times 4 \times 4)$ BM of 3D-TESH Network	49
2.30	Higher-level of 3D-TESH Network	50
2.31	BM and Higher Level of HTM Network	51
2.32	The Architecture and the Topology of Tianhe-2	54
2.33	General Architecture of Sunway TaihuLight System	56
3.1	Architecture of the BM of SCCN	64
3.2	Network-on-Chip Level (Level-2) of SCCN	66
3.3	Clarification the Circular-Shifting Idea	69
3.4	The Distance between the Groups in Level-2 Network of SCCN	70
3.5	The Bi-directional Connection between Two Nodes	72
3.6	The Routing Decision within Level-2 Network of SCCN	77
3.7	Next route within Level-2 Network of SCCN	78
3.8	Flowchart of the Routing Algorithm in Level-2	79
3.9	The structure of NoC level of Level-3 network of SCCN	82
3.10	The Board Level (Level-3) Network of SCCN	84
3.11	(8×8) Level-3 Network of SCCN	88
3.12	Routing Path between Source and Destination nodes in Level-3 Network of SCCN	94
3.13	Routing Algorithm between Two Nodes in Level-3 Network	461
3.14	Flowchart of the routing algorithm in Level-3 network	98

3.15	The Basic Module of the Cabinet Level (Level-4) of SCCN	102
3.16	The Structure of Level-4 Network of a Proposed System	103
3.17	The Routing Decision between Two Nodes within Level-4 Network	114
3.18	Routing Algorithm between Two Nodes in Level-3 Network	462
3.19	Flowchart of the routing algorithm in Level-4 network	117
3.20	The Basic Module of Level-5 Network	122
3.21	The Architecture of Level-5 Network of SCCN (System-Level)	126
3.22	Routing Decision between Two Nodes within Level-5 Network	139
3.23	The Routing Algorithm between Two Nodes within level-5	464
3.24	Flowchart of Routing Algorithm in Level-5 Network	142
4.1	Fault Diameter of the Level-1 Network of SCCN	167
4.2	Number of Paths between the source and destination nodes	184
4.3	The fault diameter of Level-2 network of SCCN	187
4.4	Arc Connectivity of Level-3 Network of a (4×4) SCCN	198
4.5	Total Number of Paths of Various Networks.	214
4.6	Fault Diameter of Level-3 Network of SCCN	216
4.7	Connectivity of Various Networks Compared to Level-4 of SCCN	244
4.8	Fault Diameter of Level-4 network of SCCN	246
4.9	Comparison of the Node Degree between Various Networks	252
4.10	Diameter Comparison of Different Networks	254
4.11	Comparison of the Average Distance between Different Networks	256
4.12	Comparison of the Cost between Various Networks	257
4.13	Arc connectivity of Various Networks	258
4.14	Bisection Width Comparison of Various Networks	261
4.15	WC comparison between different networks	264
4.16	Comparison of the packing density of various network	266

4.17	Comparison of the Message Traffic Density of Different Networks	268
4.18	Comparison of CEF of Various Networks	270
4.19	Comparison of TCEF between Various Networks	273
4.20	Comparison of the Static Cost-Effective Analysis of Different Networks	276
4.21	Comparison of the Fault Tolerance of Different Networks	278
4.22	Fault Diameter of Level-5 Network of SCCN	280
4.23	Comparison of the Fault Diameter of Various Networks	281
5.1	BM-Level of the 3D-SCCN	290
5.2	Interior and the Exterior Links in the BM-Level of the 3D-NoC Level	294
5.3	Architecture of the 3D-NoC Level of SCCN	297
5.4	Routing Protocol of the 3D-NoC Level of SCCN	306
5.5	Routing Algorithm for the 3D-NoC Level of SCCN	307
5.6	Flowchart of Routing Algorithm in the 3D-NoC Level of SCCN	309
5.7	BM of the Level-2 Network of the 3D-SCCN	314
5.8	Level-2 of the 3D-SCCN Network	316
5.9	Routing Decision between Two Nodes in the Level-2 of the 3D-SCCN	328
5.10	Routing Algorithm between Two Nodes in the Level-2 of the 3D-SCCN	332
5.11	Flowchart of the Routing Algorithm in Level-2 of the 3D-SCCN	334
5.12	BM of the Level-3 of the 3D-SCCN	338
5.13	Level-3 Network of the 3D-SCCN	343
5.14	Routing Decision in the 3D-Level-3 Network of SCCN	356
5.15	Routing Algorithm between Two Nodes within the Level-3 Network of the 3D-SCCN	361
5.16	Flowchart of the Routing Algorithm in Level-3 of the 3D-SCCN	363
6.1	Fault Diameter of the 3D-NoC Level of SCCN	386

6.2	Fault Diameter of Level-2 Network of the 3D-SCCN	408
6.3	Node Degree Comparison of Different Networks	412
6.4	Network Diameter Comparison of Different Networks	413
6.5	Cost Comparison of Different Networks	414
6.6	Average Distance Comparison between Various Networks	416
6.7	Arc Connectivity Comparison of Various Networks	417
6.8	BW Comparison of Different Networks	419
6.9	Wiring Complexity Comparison of Various Networks	422
6.10	Packing Density of Various Networks	423
6.11	Message Traffic Density Comparison of Various Networks	425
6.12	CEF of Different Networks	428
6.13	TCEF of Different Networks	429
6.14	Static Cost-effective Analysis of Various Networks	432
6.15	Fault Tolerance Comparison between Several Networks	435
6.16	Fault Diameter of Level-2 of the 3D-SCCN	437
6.17	Fault Diameter Comparison of Various Networks	437

LIST OF ABBREVIATIONS

SCCN	Shifted Completely Connected Network
MPC	Massively Parallel Computer
PEs	Processing Elements
HINs	Hierarchical Interconnection Networks
NoC	Network-on-Chip
VLSI	Very Large-Scale Integration
CPUs	Central Processing Units
SoC	System on Chip
2D-Mesh	Two-Dimensional Mesh
2D-Torus	Two-Dimensional Torus
TESH	Tori Connected Mesh
TTN	Tori Connected Torus Network
HTN	Hierarchical Torus Network
THIN	Triple-based hierarchical interconnection network
BSN	Block Shift Network
STTN	Symmetric Tori Connected Torus Network
3D ICs	Three-Dimensional Integrated Circuits
3D	Three-Dimensional
2D	Two-Dimensional
3D-Mesh	Three-Dimensional Mesh Network
3D-Torus	Three-Dimensional Torus Network
H3DM	Hierarchical 3D-Mesh Network
BM	Basic Module
H3DT	Hierarchical 3D-Torus Network
MH3DT	Modified Hierarchical 3D-Torus Network
3D-TESH	Hierarchical 3D Tori Connected Mesh
HTM	Hierarchical Tori Connected Mesh
NUDT	National University of Defense Technology
MIC	Many-Integrated-Core
CPEs	Computing Processing Elements
NRCPC	National Research Center of Parallel Computer Engineering and Technology
MPEs	Management Processing Elements
MC	Memory Controllers
SI	System Interface
ICs	Integrated Circuits
CGs	Core Groups
2D-SCCN	2D-Shifted Completely Connected Network
3D-SCCN	3D-Shifted Completely Connected Network
BW	Bisection Width
WC	Wiring Complexity
CEF	Cost Effective Factor
CE	Cost-Effectiveness
TCEF	Time-Cost Effectiveness Factor
3D-NoC	3D Network-on-Chip

CHAPTER ONE

INTRODUCTION

1.1 BACKGROUND OF THE STUDY

At the current time, technological advancements arose in various areas such as Artificial intelligence, Machine learning, big data, Internet of Things (IoT), autonomous robots and vehicles. Therefore, the need for super-fast systems to compute massive amounts of data in a short time increased. As a result, Massively Parallel Computer (MPC) Systems emerged to deal with the high demand of technology and to solve complicated problems in parallel by dividing the problem into parts and distribute them between thousands of CPUs and combine their results to produce an optimal and fast solution. The importance of these systems elevated because it provides power to collect, organize, and analyze big amounts of data to improve the modern life of humankind. For instance, these systems used to develop new sources of energy, improve healthcare by developing new medicines, predict and mitigate disasters, forecast weather, and many beneficial uses (Awal et al., 2014; Rahman et al., 2012) Using a single CPU core to build a computer system, make it difficult on this system to cope with the high demand of signaling technology. Moreover, sequential computers reached maximum limits to overcome many current computing problems (Sarkar, 1993; Al Faisal et al., 2016; Rahman et al., 2011). Therefore, finding an alternative solution was the priority of the research community to fulfil the new technology requirements by creating MPC systems with multiprocessor cores to replace the sequential ones. These systems considered as the high-level computer systems and used to model many difficult

problems in many areas including engineering and science (Barney, 2010). Improve the performance and reduce the cost of MPC systems is the priority of the research work. Therefore, many designs of MPC systems presented looking for an ideal one (Awal et al., 2014; Rahman et al., 2012).

The underlying interconnection network is a backbone of MPC system; these networks responsible for interconnecting the processing elements (PEs) inside the system, and it has a vital role in either improving or degrading the cost and the performance of these systems. The cost depends on the price of network devices and wires. Therefore, many research works focus on improving the performance of these networks by presenting different topologies to arrange and manage the connection between the PEs inside the system (Kim et al., 2008). The performance of these topologies evaluates based on a group of static and dynamic performance parameters to test and compare them to other topologies to find an optimal topology to be used in designing MPC systems, thus, many topologies have been proposed for this purpose. (Ali et al., 2016). Expanding the interconnection network size by increasing the number of computing nodes is the most important factor in strengthening the computing power of the system to overcome the increasing demand for computational power. The early structures of interconnection network topologies showed poor performance with the increase of the network size. Therefore, to cope with this problem, hierarchical interconnection networks (HINs) have been proposed to be an alternative solution to replace the conventional networks in building MPC systems. These networks proved their capability in increasing computing nodes number in the system to millions of nodes. Furthermore, it is an affordable way to be used in building MPC systems, and it proved proficiency in reducing power consumption. Th Therefore, a diversity of

hypercube based on hierarchical interconnection networks (HINs) proposed. However, expanding the size of these networks by adding more nodes caused large numbers of physical links and make it excessively large. To avoid this problem, numerous k-ary n-cube networks based on HINs presented such as 3D-Mesh, 3D-torus, TESH, and Cube Connected Cycles networks, however, the throughput of these networks is still very low (Al Faisal et al., 2016; Rahman et al., 2010; Rahman et al., 2009).

The rapid improvements of Very-Large-Scale-Integration (VLSI) design created a suitable environment to place a complete system in a single chip. Network-on-Chip (NoC) is an interconnection network used to connect many cores inside one chip presented as a single silicon chip to employ the communication structures of large-scale to very-large-scale integration systems (Rahman et al., 2009; Ali et al. 2016). Besides, it used to improve the communication between processors and memories inside the chip by replacing the buses and ad-hock wiring solutions of a single-core chip (Kim et al., 2005). NOC is predicted to have a promising future in improving the performance and the architecture of the future of MPC systems (Amano, 2013). The benefits of using NoC in designing large-scale systems reduce system wires complexity, control power, and provide a reliable system. The design of NoC allows the messages to flow from a source node to a destination node through numerous links that involve routing decisions at switches. Also, NoC handles synchronization issues better than the other designs. Furthermore, it provides higher operating frequencies and provides easier verification of problems due to the good design of these networks (Anagnostopoulos et al., 2009; Miura et al., 2013; Ali et el., 2016). The performance of NoC is affected by the design of the network topology which in turn affects the performance and the cost of MPC systems. Besides, the correct choice of routing protocol is important in decreasing the

network latency and congestion (Anagnostopoulos et al., 2009). Besides, the significance of hierarchical interconnection networks (HINs) is in maintaining the system performance with a high number of nodes due to its role in providing a cost-effective network. All these reasons motivated this research to propose a new topology of a hierarchical interconnection network to be as a basic module (BM) to build future generations of MPC systems. In this thesis, we will propose an architecture of a hierarchical interconnection network (HIN); this network is a completely connected network presented to enhance the performance of MPC systems. Shifted completely connected network (SCCN) is a new design of a proposed topology for Network-on-Chip (NoC) which will interconnect hierarchically to create a complete MPC system.

1.2 STATEMENT OF THE PROBLEM

The Increase of computing power and network bandwidth due to the advancements in signaling technology have motivated the researchers to find an alternative solution with special characteristics able to model complex problems in many areas (Kim et al., 2008 Development of sequential computer systems exhausted their capacity (Al Faisal et al., 2016). Therefore, to exploit the huge computing power, and yield benefits of parallelism in solving problems, supercomputers with a high number of nodes became a necessity to support technology developments of in many areas. Many problems need to be solved to build an optimum computing system. Thereby, the motivation for this research are the following problems:

1) Expand the interconnection network with thousands or millions of nodes is an infeasible with conventional interconnection networks, due to large diameter